

What is claimed is:

1 1. A deep trench self-alignment process for an active
2 area of a partial vertical cell, comprising:
3 providing a semiconductor substrate having two deep
4 trenches;
5 forming a deep trench capacitor in each deep trench, lower
6 than the top surface of the semiconductor substrate;
7 forming an isolating layer covering each deep trench
8 capacitor;
9 filling a mask layer in each deep trench;
10 forming a photoresist layer covering the semiconductor
11 substrate between the deep trenches, wherein the
12 mask layer surface is partially covered by the
13 photoresist layer;
14 etching the semiconductor substrate using the photoresist
15 layer and the mask layers as etching masks to below
16 the isolating layer; and
17 removing the photoresist layer and the mask layers,
18 wherein the pillared semiconductor substrate
19 between the deep trenches act as an active area.

1 2. The deep trench self-alignment process for an active
2 area of a partial vertical cell of claim 1, wherein a ring-shaped
3 insulating layer is formed on a top sidewall of each deep trench.

1 3. The deep trench self-alignment process for an active
2 area of a partial vertical cell of claim 2, wherein the
3 ring-shape insulating layer is a collar oxide layer.

1 4. The deep trench self-alignment process for an active
2 area of a partial vertical cell of claim 1, wherein the isolating
3 layer is an oxide layer.

1 5. The deep trench self-alignment process for an active
2 area of a partial vertical cell of claim 1, wherein the mask
3 layer is an anti-reflection coating layer.

1 6. The deep trench self-alignment process for an active
2 area of a partial vertical cell of claim 1, wherein the etching
3 is carried out using a gas mixture containing HBr and oxygen.

1 7. The deep trench self-alignment process for an active
2 area of a partial vertical cell of claim 1, wherein the etching
3 is anisotropic.

1 8. The deep trench self-alignment process for an active
2 area of a partial vertical cell of claim 8, wherein the
3 anisotropic etching is plasma or reactive ion etching.

1 9. A deep trench self-alignment process for an active
2 area of a partial vertical cell, comprising:

3 providing a semiconductor substrate, wherein a pad layer

4 is formed covering the semiconductor substrate;

5 forming two deep trenches in the semiconductor substrate

6 separated by a predetermined distance;

7 forming a deep trench capacitor in each deep trench,

8 wherein the deep trench capacitors are below the

9 top surface of the semiconductor substrate, and a

10 ring-shaped insulating layer is formed on a top

11 sidewall of each deep trench;

12 conformally forming an isolating layer covering the
13 semiconductor substrate and the deep trenches;
14 removing the isolating layer from the sidewall of the
15 deep trench to leave the isolating layer on the deep
16 trench capacitor;
17 forming a mask layer covering the semiconductor
18 substrate, wherein the deep trench is filled with
19 the mask layer;
20 planarizing the mask layer until the semiconductor
21 substrate is exposed to leave the mask layer in the
22 deep trenches;
23 forming a photoresist layer covering the semiconductor
24 substrate between the deep trenches, wherein the
25 mask layer is partially covered by the photoresist
26 layer;
27 etching the semiconductor substrate to a predetermined
28 depth using the photoresist layer and the mask layer
29 as etching masks; and
30 removing the photoresist layer and the mask layer, wherein
31 a pillared semiconductor substrate between the deep
32 trenches act as an active area.

1 10. The deep trench self-alignment process for an active
2 area of a partial vertical cell of claim 9, wherein the pad
3 layer is a pad oxide layer or a pad nitride layer.

1 11. The deep trench self-alignment process for an active
2 area of a partial vertical cell of claim 9, wherein the
3 predetermined distance between the deep trenches is about 1200
4 to 1400Å.

1 12. The deep trench self-alignment process for an active
2 area of a partial vertical cell of claim 9, wherein the
3 ring-shape insulating layer is a collar oxide layer.

1 13. The deep trench self-alignment process for an active
2 area of a partial vertical cell of claim 9, wherein the isolating
3 layer is an oxide layer.

1 14. The deep trench self-alignment process for an active
2 area of a partial vertical cell of claim 9, wherein removal
3 uses anisotropic etching.

1 15. The deep trench self-alignment process for an active
2 area of a partial vertical cell of claim 9, wherein the mask
3 layer is an anti-reflection coating layer.

1 16. The deep trench self-alignment process for an active
2 area of a partial vertical cell of claim 9, wherein planarization
3 uses chemical mechanical polishing or etching.

1 17. The deep trench self-alignment process for an active
2 area of a partial vertical cell of claim 9, wherein the etching
3 is carried out using a gas mixture containing HBr and oxygen.

1 18. The deep trench self-alignment process for an active
2 area of a partial vertical cell of claim 9, wherein the etching
3 is anisotropic.

1 19. The deep trench self-alignment process for an active
2 area of a partial vertical cell of claim 18, wherein the
3 anisotropic etching is plasma etching or reactive ion etching.

1 20. The deep trench self-alignment process for an active
2 area of a partial vertical cell of claim 9, where the
3 predetermined depth is about 2600 to 3000Å.